

# Chip Level Modeling With Vhdl By James R. Armstrong

**By James R. Armstrong**

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He was a member of the original IEEE standardization committee; authored Chip Level Modeling With VHDL, By James R. Armstrong, F. Gail Gray;

<http://www.informit.com/authors/bio/5ea2ca58-5bc7-4305-8a0f-5adac5484f47>

JAMES R. ARMSTRONG and DR. F. GAIL GRAY are Professors of Electrical and Computer Engineering at Virginia Tech. Dr authored Chip Level Modeling With VHDL,

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JAMES R. ARMSTRONG and DR. F. GAIL GRAY are Professors of Electrical and Computer Engineering at Virginia Tech. Dr authored Chip Level Modeling With VHDL,

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James R. Armstrong is the author of VHDL Design Representation and Synthesis (4.50 avg rating, 4 ratings, 0 reviews, published 2000), Chip Level Modeling [http://www.goodreads.com/author/show/677325.James\\_R\\_Armstrong](http://www.goodreads.com/author/show/677325.James_R_Armstrong)

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(VHSIC Hardware Description Language) A comparison of the coding styles between the RTL modeling and Algorithm level Modeling a real industry chip <http://esd.cs.ucr.edu/labs/tutorial/>

Chip-level modeling with VHDL. Author: James R. Armstrong: Virginia Polytechnic Institute and State Univ. Publication: Book: Chip-level modeling with VHDL : <http://dl.acm.org/citation.cfm?id=49146&prelayout=tabs>

The IEEE Standard 1076 defines the VHSIC Hardware Description Language or when a VHDL model is translated into the VHDL for use with their chips, [http://en.wikipedia.org/wiki/VHSIC\\_hardware\\_description\\_language](http://en.wikipedia.org/wiki/VHSIC_hardware_description_language)

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