

# Chip Level Modeling With Vhdl By James R. Armstrong

**By James R. Armstrong**

## **A Fault Model for VHDL Descriptions at the - -**

by James R Armstrong, Fong-Shek Lam, Paul C Ward The faults have been injected on a chip-level VHDL model, using an injection tool desig

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The IEEE Standard 1076 defines the VHSIC Hardware Description Language or when a VHDL model is translated into the VHDL for use with their chips,

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Rapid Development and Testing of Behavioral Models Armstrong, J. R., Chip-Level Modeling with and W. R. Cyre, Generation of VHDL Models from Informal

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He was a member of the original IEEE standardization committee; authored Chip Level Modeling With VHDL, By James R. Armstrong, F. Gail Gray;

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Making Verilog models compatible with VHDL VITAL level 0 models by Yuri Tatarnikov, SEVA Technologies modeling PCB interconnect delays as chip port delays.

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### **Pearson - VHDL Design Representation and -**

VHDL Design Representation and Synthesis, 2/E James R. Armstrong, Virginia Polytech Institute F. Gail Gray, Virginia Polytech Institute  
productFormatCode=P01

### **A high- level language for design and modeling of -**

The IEEE standard language for description of hardware is VHDL. J. R. Armstrong, Chip-Level Modeling with VHDL, Prentice-Hall, Englewood Cliffs, New Jersey,

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Chip Level Modelling with VHDL, : James R. Armstrong, Prentice Hall Amazon. .

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## **Fault Injection into VHDL Models: Experimental -**

Fault Injection into VHDL Models: James R. Armstrong, Chip-level modeling with VHDL, Prentice-Hall, Inc., Upper Saddle River, NJ, 1988 : 25

## **James R. Armstrong (Author of VHDL Design - -**

James R. Armstrong is the author of VHDL Design Representation and Synthesis (4.50 avg rating, 4 ratings, 0 reviews, published 2000), Chip Level Modeling

## **Timing Constraint Checks in VHDL a comparative -**

Armstrong J.R.:Chip Level Modeling with VHDL, Prentice-Hall, 1989. [3] Dubois J-L, Liu F., Pawlak A.: Standard Component Modeling with VHDL, Proc. of ASIM 91.

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